List of Publications
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I. Book Chapters

(104) **Functionality-Enhanced Devices: An alternative to Moore's Law**
Chapter 3 "Germanium based nanowire polarity controllable transistor"
W. M. Weber , J. Trommer, A. Heinzig and T. Mikolajick
Editor: P. E. Gaillardon
The Institution of Engineering and Technology (IET), Hertfortshire UK (2018)
ISBN: 9781785615580

(103) **Silicon Nanowires: Fabrication and Applications** in **Anisotropic Materials:**
Chapter 1 Preparation, Properties and Applications
T. Mikolajick and W. M. Weber, Editor: L. Quan
Springer International Publishing pp. 1-25 (2015)
ISBN: 978-3-319-18292-6

II. Review and Overview Papers
— Peer Reviewed —

(102) **Silicon and Germanium Nanowire Electronics: Physics of Conventional and Unconventional Transistors**
W. M. Weber and T. Mikolajick
Reports on Progress in Physics (ROPP) **80,** 066502 (50pp) (2017)
DOI: 10.1088/1361-6633/aa56f0

(101) **The RFET - a reconfigurable nanowire transistor and its application to novel electronic circuits and systems**
T. Mikolajick , A. Heinzig, J. Trommer, T.Baldauf and W. M. Weber
Semiconductor Science and Technology SST **32**, 043001 (17pp), (2017)
DOI: 10.1088/1361-6641/aa5581

(100) **Current Progress in the Chemical Vapor Deposition of Type-Selected Horizontally Aligned Single Wall Carbon Nanotubes**
I. Ibrahim, T. Gemming, W. M. Weber, T. Mikolajick, Z. Liu and M. J. Rümmeli
ACS Nano **10** pp 7248–7266 (2016)

III. Peer-Reviewed Publications & Conference Publications with Scientific Quality Assurance

— 2020 —

(99) Top-down fabricated reconfigurable FET with two symmetric and high-current on-states
M. Simon, B. Liang, D. Fischer, M. Knaut, A. Tahn, T. Mikolajick and W. M. Weber
IEEE Electron Device Letters Accepted Manuscript Mai 2020

(98) Inherent Charge-Sharing-Free Dynamic Logic Gates Employing Transistors with Multiple Independent Inputs
J. Trommer, M. Simon, S. Slesazeck, W. M. Weber and T. Mikolajick
IEEE Journal of the Electron Devices Society, In Press 2020
DOI**:** 10.1109/JEDS.2020.2986940

(97) A silicon nanowire ferroelectric field-effect transistor
V. Sessi, M. Simon, H. Mulaosmanovic, D. Pohl, M. Loeffler, T. Mauersberger, F. P. G. Fengler, T. Mittmann, C. Richter, S. Slesazeck, T. Mikolajick, and W. M.Weber
Advanced Electronic Materials **vol. 6** (4) 1901244, 2020. DOI: https://doi.org/10.1002/aelm.201901244

(96) Size effect of electronic properties in highly arsenic-doped silicon nanowires
T. Mauersberger, I. Ibrahim, M. Grube A. Heinzig, T. Mikolajick, W. M.Weber
Soild State Electronics 168, 107724 (2020) DOI: 10.1016/j.sse.2019.107724

(95) Surface related differences between uncoated versus carbon-coated Silicon Nanowire Electrodes on performance in Lithium Ion Batteries
A. Krause, U. Langklotz, D. Pohl, O. Tkacheva, T. Mikolajick, D. Pohl, K. Nielsch, W. M. Weber
Journal of Energy Storage **27**, p. 101052 (2020) DOI: 10.1016/j.est.2019.101052

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(94) Eliminating Charge Sharing in Clocked Logic Gates on the Device Level Employing Transistors with Multiple Independent Inputs
J. Trommer, M. Simon, S. Slesazeck, W. M. Weber and T. Mikolajick
IEEE ESSDERC Proc. pp. 134-137. (2019) DOI: 10.1109/ESSDERC.2019.8901730

(93) IPCEI Subcontracts Contributing to 22-FDX Add-on Functionalities at GF
S. Kolodinski, C. Mart, W. Weinreich, V. Sessi, J. Trommer, T. Chohan, H. Mulaosmanovic, W. M. Weber, S. Slesazeck, B. Peng., C. Esposito, Y. Zimmermann, M. Schröter, Xin Xu, P.V. Testa, C. Carta, F. Ellinger, S. Lehmann, M. Drescher and M. Wiatr

IEEE ESSDERC Proc. pp. 74-77 (2019) DOI: 10.1109/ESSDERC.2019.8901736

(92) Towards Reconfigurable Electronics: Silicidation of Top-Down Fabricated Silicon Nanowires
MB Khan, D Deb, J Kerbusch, F Fuchs, M Löffler, S Banerjee, U Mühle, F. Fuchs, M. Löffler, S. Banerjee, U. Mühle, W. M Weber, S. Gemming, J. Schuster, A. Erbe, Y.M Georgiev
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(91) In Situ Raman Spectroscopy on Silicon Nanowire Anodes Integrated in Lithium Ion Batteries
A. Krause, O. Tkacheva, A. Omar, U. Langklotz, L. Giebeler, S. Dörfler, F Fauth, T. Mikolajick, W. M Weber
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(90) Designing Efficient Circuits Based on Runtime-Reconfigurable Field-Effect Transistors
S. Rai, J. Trommer, M. Raitza, T. Mikolajick, W. M. Weber, and A. Kumar
IEEE TRANSACT. ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, **27** (3) pp. 560 – 572 (2019)
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(89) Size effect of electronic properties in highly arsenic-doped silicon nanowires
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T. Baldauf, A. Heinzig, T. Mikolajick and W. M. Weber
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(87) Junction tuning by ferroelectric switching in silicon nanowire Schottky field effect transistors
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(86) Gating Hysteresis as an Indicator for Silicon Nanowire FET Biosensors
B. Ibarlucea, L. Römhildt, F. Zörgiebel, S. Pregl, M. Vahdatzadeh, W. M. Weber, T. Mikolajick, J. Opitz, L. Baraban and G. Cuniberti
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(85) A wired-AND transistor: Polarity controllable FET with multiple inputs
M. Simon, J. Trommer, B. Liang, D. Fischer, T. Baldauf, M. B. Khan, A. Heinzig, M. Knaut, Y. M. Georgiev, A. Erbe, J. W. Bartha, T. Mikolajick and W. M. Weber
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(84) A Physical Synthesis Flow for Early Technology Evaluation of Silicon Nanowire based Reconfigurable FETs
S. Rai, A. Rupani, D. Walter, M. Raitza, A. Heinzig, T. Baldauf, J. Trommer, C. Mayr, W. M. Weber and A. Kumar
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(83) Reconfigurable Si Nanowire Nonvolatile Transistors
S.-J. Park, D.-Y. Jeon, S. Piontek, M. Grube, J. Ocker, V. Sessi, A. Heinzig, J. Trommer, G.-T. Kim, T. Mikolajick and W. M. Weber
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(81) Reconfigurable NAND-NOR Circuits Fabricated by a CMOS Printing Technique
A. Heinzig, S. Pregl, J. Trommer, T. Mikolajick and W. M. Weber
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(80) Human α-thrombin detection platform using aptamers on a silicon nanowire field-effect transistor
L. Römhildt, F. Zörgiebel, B. Ibarlucea, M. Vahdatzadeh, L. Baraban, G. Cuniberti, S. Pregl, W. M Weber, T. Mikolajick and J. Opitz
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(77) In-Depth Electrical Characterization of Carrier Transport in Ambipolar Si-NW Schottky-Barrier FETs
D.Y. Jeon, T. Baldauf, S. J. Park, S. Pregl, L. Baraban, G. Cuniberti, T. Mikolajick and W. M. Weber
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J. Trommer, A. Heinzig, U. Mühle, M. Löffler, A. Winzer, P. M. Jordan, J. Beister, T. Baldauf, M. Geidel, B. Adolphi, E. Zschech, T. Mikolajick, and W. M. Weber
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(73) Exploiting transistor-level reconfiguration to optimize combinational circuits
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T. Baldauf, A. Heinzig, J. Trommer, T. Mikolajick, W.M. Weber
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(70) Integrating Bottom-Up Grown Silicon Nanowires on a CMOS Chip to Realize High-Density Transistor Arrays for Chemical Sensing
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(67) Printable Parallel Arrays of Si Nanowire Schottky-Barrier-FETs with Tunable Polarity for Complementary Logic
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(63) TEM Study of Schottky Junctions in Reconfigurable Silicon Nanowire Devices
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(60) Scaling and graphical transport-map analysis of ambipolar Schottky-barrier thin-film transistors based on a parallel array of Si-nanowires
D.-Y. Jeon, S. Pregl, S.-Y. Park, L. Baraban, G. Cuniberti, T. Mikolajick and W. M. Weber
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(52) A multi-Optoelectronic Switching of Nanowire - based Hybrid Organic/Oxide/Semiconductor Field - Effect Transistors

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(51) Ionic effects on the transport characteristics of nanowire-based FETs in a liquid environment

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(49) A multi-spectroscopic and microscopic characterization of graphene on single crystal Ir(111) films on Si(111) wafers

C. Struzzi, N.I. Verbitskiy, A.V. Fedorov, A. Nefedov, O. Frank, M. Kalbac, G. Di Santo, M. Panighel, A. Goldoni, J. Gärtner, W. Weber, M. Weinl, M. Schreck, Ch. Wöll, H. Sachdev, A. Grüneis, L. Petaccia
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(48) Development of nanowire devices with quantum functionalities

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(44) Reconfigurable Silicon Nanowire Devices and Circuits: Opportunities and Challenges

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T. Mikolajick, A.Heinzig, J. Trommer, S. Pregl, M. Grube, G. Cuniberti and W. M. Weber
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(35) **Reconfigurable silicon nanowire transistors**
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W. M. Weber, A. Heinzig and T. Mikolajick
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M. Grube, D. Martin, W. M. Weber, O. Bierwagen, T. Mikolajick, L. Geelhaar and H. Riechert
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(25) Evaluation of the electrical and physical properties of thin calcium titanate high-*k* insulators for capacitor applications
A.Krause,W.M. Weber, A. Jahn, K. Richter, D. Pohl, B. Rellinghaus, U. Schröder, J. Heitmann and T.Mikolajick
Journal of Vacuum Science and Technology B **29**, 01AC07 (2011)

(24) Reduction of leakage currents with nanocrystals embedded in an amorphous matrix in metal-insulator-metal capacitor stacks
A. Krause, W. M. Weber, U. Schröder, D. Pohl, B. Rellinghaus, J. Heitmann and T. Mikolajick
Applied Physics Letters **99**, 222905 (2011)

– 2010 –

(23) Influence of composition and bottom electrode properties on the local conductivity of TiN/HfTiO$_2$ and TiN/Ru/HfTiO$_2$
D. Martin, M. Grube, P. Reinig, L. Oberbeck, J. Heitmann, W. M. Weber, T. Mikolajick and H. Riechert.
Applied Physics Letters **98**, 012901 (2010)

(22) An investigation of the electrical properties of MIS capacitors with pyrolytic carbon electrodes
A.P. Graham, C.Richter, T. Jay, W. Weber, S. Knebel, U. Schroeder and T.Mikolajick
Journal of Applied Physics **108**, 104508 (2010)

(21) Direct comparison of catalyst-free and catalyst-induced GaN nanowires
C. Chéze, L. Geelhaar, O. Brandt, W. M. Weber, H. Riechert S. Münch, R. Rothemund, S. Reitzenstein, A. Forchel, T. Kehagias, P. Kominou, G. P. Dimitrakopulos and T. Karakostas.
Nano Research **3 pp. 528-536 (2010)**

(20) An investigation of the electrical properties of pyrolytic carbon in reduced dimensions; vias and wires
A.P. Graham, G. Schindler, G.S. Duesberg, T. Lutz and W. Weber
Journal of Applied Physics **107**, 114316 (2010)

— 2009 —

(19) Local charge transport in nanoscale amorphous and crystalline regions of high-k $(ZrO_2)_{0.8}(Al_2O_3)_{0.2}$ thin films
D. Martin, M. Grube, W. M. Weber, J. Rüstig, O. Bierwagen, L. Geelhaar and H. Riechert.
Applied Physics Letters **95** p. 142906 (2009)

(18) Investigation of zirconium oxide based high-k dielectrics for future memory applications
M. Grube, D. Martin, W. M. Weber, O. Bierwagen, L. Geelhaar and H. Riechert.
****** Invited paper:*** *IEEE Proc. Semiconductors Circuits and Systems Conference 2009* (2009)

— 2008 —

(17) Tuning the Polarity of Si-Nanowire Transistors Without the Use of Doping
W. M. Weber, L. Geelhaar, L. Lamagna, M. Fanciulli, F. Kreupl, E. Unger, H. Riechert, G. Scarpa and P. Lugli.
IEEE Proc. on Nanotechnology 2008, pp. 580-581 (2008)

— 2007 —

(16) Axial and radial growth of Ni-induced GaN nanowires
L. Geelhaar, C. Chèze, W. M. Weber, R. Averbeck, H. Riechert, Th. Kehagias, Ph. Komninou, G. P. Dimitrakopulos, and Th. Karakostas.
Applied Physics Letters **91**, p. 093113 (2007)

(15) Silicon to nickel-silicide axial nanowire heterostructures for high performance electronics
W. M. Weber, L. Geelhaar, E. Unger, C. Chèze, F. Kreupl, H. Riechert and P. Lugli.
****** Invited Paper ***** *XXI. IWPENM proceedings* 2007.
physica status solidi (b) **244**, pp. 4170-4175 (2007).

(14) Analysis of the hysteretic behavior of silicon nanowire transistors
Z. Fahem, G. Csaba, C. M. Erlen, P. Lugli, W. M. Weber, L. Geelhaar and H. Riechert.
physica status solidi (c) HCIS proceedings (2007)

(13) Fabrication of a nano-scale NAND memory array based on a SONOS Fin-FET cell using e-beam lithography and hydrogen-silesquioxane resist
T. Lutz, M. Specht, L. Risch, C. Friederich, L. Dreeskornfeld, J. Kretz, W. Weber and W. Rösner.
Microelectronic Engineering **84** pp. 1578-1580 (2007)

— 2006 —

(12) Silicon-nanowire transistors with intruded nickel-silicide contacts
W. M. Weber, L. Geelhaar, A. P. Graham, E. Unger, G. S. Duesberg, M. Liebau, W. Pamler, C. Cheze, H. Riechert, P. Lugli and F. Kreupl.
Nano Letters **6, pp. 2660-2666 (2006)**

(11) Non-linear gate length dependence of on-current in Si-Nanowire FETs
W. M. Weber, A. P. Graham, G. S. Duesberg, M. Liebau, C. Cheze, L. Geelhaar, E. Unger, W. Pamler, W. Hoenlein, H. Riechert, F. Kreupl, P. Lugli.
IEEE 36th ESSDERC proceedings pp. 423-426 (2006)

(10) Multi-level p+ tri-gate SONOS NAND string arrays
C. Friederich, M. Specht, T. Lutz, F. Hoffmann, L. Dreeskornfeld, W. M. Weber, J. Kretz, T. Melde, W. Roesner, E. Landgraf, J. Hartwich, M. Staedele, Risch, and D. Richter.
***IEDM (International Electron Devices Meeting)Int. Tech. Digest*. – *IEEE* (2006)**

(9) Silicon nanowires: catalytic growth and electrical characterization
W. M. Weber, G. S. Duesberg, A. P. Graham, M. Liebau, E. Unger, C. Chèze, L. Geelhaar, P. Lugli, H. Riechert and F. Kreupl.
****** Invited Paper ***** *XX. IWPENM Proceedings (2006)*
physica status solidi (b) **243**, pp. 3340-3345 (2006)

— 2005 —

(8) Electron beam lithography for nanometer-scale planar double-gate transistors
W. M. Weber, G. Ilicali, J. Kretz, L. Dreeskornfeld, W. Rösner, W. Hansch and L. Risch.
Microelectronic Engineering **78**, pp. 206-211 (2005)

(7) Comparative study of calixarene and HSQ resist systems for the fabrication of sub 20nm MOSFET device demonstrators
J. Kretz, L. Dreeskornfeld, G. Ilicali, T. Lutz, and W. M. Weber.
Microelectronic Engineering **78** , pp. 479-483 (2005)

(6) Fabrication of ultra-thin-film SOI transistors using the recessed channel concept
L. Dreeskornfeld, J. Hartwich, F. Hofmann, J. Kretz, E. Landgraf, R.J. Luyken, W. Rösner, R. Schröter, T. Schulz, M. Specht, M. Städele, W. M. Weber and L. Risch
Microelectronic Engineering **78–79**, 224–228 (2005)

(5) Planar Double Gate Transistors with Asymmetric Independent Gates
G. Ilicali, W. Weber, W. Roesner, L. Dreeskornfeld, J. Hartwich, J. Kretz, T. Lutz, J.-P- T. Mazellier, M. Stadele, M. Specht, J. R. Luyken, E. Landgraf, F. Hofmann, L. Risch, R. Kasmaier and W. Hansch
2005 Proc. IEEE International SOI Conference, pp. 126-127 (2005)

— 2004 —

(4) Novel dual bit tri-gate charge-trapping memory devices
M. Specht, R. Kömmling, F. Hofmann, V. Klandzievski, L. Dreeskornfeld, W. Weber, J. Kretz, E. Landgraf, T Schulz, J. Hartwich, W. Rösner, M. Städele, R.J. Luyken, H. Reisinger, A. Graham, E. Hartmann and L. Risch.
Electron Device Letters **(IEEE) 25, p. 810 (2004)**

(3) Sub-40nm tri-gate charge trapping nonvolatile memory cells for high-density applications
M. Specht, R. Kömmling, L. Dreeskornfeld, W. Weber, F. Hofmann, D. Alvarez, J. Kretz, R. J. Luyken, W. Rösner, H. Reisinger, E. Landgraf, T. Schulz, J. Hartwich, M. Städele, V. Klandievski, E. Hartmann and L. Risch.
VLSI Tech. Digest **- IEEE pp. 244-245 (2004)**

(2) Recessed Channel SOI Transistors
L. Dreeskornfeld, J. Hartwich, J. Kretz, R. Schröter, W. Weber, et al.
The Electrochemical Soc. Proc. Intl. Conf. on Semiconductor Technology ECS ISTC2004 p. 311 (2004)

(1) Use of LPCVD TEOS as a direct bonding material for layer transfer: densified vs. undensified
G. Ilicali, W. Rösner, W. Weber, S. Boz, L. Dreeskornfeld, J. Hartwich, J. Kretz, J. R. Luyken, E. Landgraf, F. Hofmann,L. Risch and W. Hansch
2004 Proc. IEEE International SOI Conference, pp. 44 – 45 (2004)

IV. Invited Conference Talks

(26) Nanowire Innovations from Devices to Circuits
MESS 2020 Vienna
Postponed to 2021 due to COVID-19 shutdown

(25) Nanowire metal -semiconductor heterostructures for functionality enhancement and quantum transport
Workshop and Symposium on Schottky Barrier MOS (SB-MOS) devices and IEEE EDS Mini-Colloquium on "Non-conventional Devices and Technologies
Postponed to 30.9.2020-1.10.2020 due to COVID-19 shutdown
Giessen, Germany, Inviter: Dr. Mike Schwarz

(24) Nanowire Schottky devices
W. M. Weber
Symposium on Schottky barrier MOS devices - "devil or savior" Darmstadt, Germany 7.8.2018
Inviters: Dr. Mike Schwarz, Prof. Schwalke

(23) Semiconductor nanowire electronics and their prospects within the cluster of excellence cfaed
Keynote Lecture at the Nanonet Seminar 2018, Dresden, Germany
Mai 24. 2018
Inviter: Dr. rer. nat. habil. Peter Zahn

(22) Group IV nanowires for beyond CMOS circuits and energy storage
W. M. Weber
Freiberger Silicon Days, Freiberg, Germany
June 6. 2017
Inviter: Prof. Johannes Heitmann

(21) High-Yield Silicon and Germanium Nanowire Printed Transistors and Logic Circuits
Keynote Lecture: Pacific Rim Meeting PRiME 2016 / ECS Meeting
W. M. Weber
02-07 October 2016 Honolulu, USA

(20) Advances in energy storage by integrating Silicon nanowires to Li based battery systems
International Conference on Small Science ICSSCI 2015- Symposium on Energy Materials
M. Grube, A. Krause, W. M. Weber, T. Mikolaijik, S. Dörfler, M. Piwko, T. Jaumann, F. M. Wisser, U. Langklotz
8-11 November 2015 Thailand

(19) The RFET – a reconfigurable nanowire transistor and the realization of novel CMOS circuits
A. Heinzig, J. Trommer, T. Baldauf, T. Mikolajick and W. M. Weber
E-MRS Fall Meeting, Warsaw-Poland
16 September 2015
Inviter: Prof. Dirk König (University of New South Wales)

(18) Highly Cyclable Nanowire Anodes for Li-ion and Li-S Batteries
2015 Energy-Materials and -Nanotechnology East Meeting, Beijing, China
W. M. Weber et al.
20-23 April 2015

(17) Anisotropic Nickel Silicidation in Nanoscale Dimensions
2015 MAM – IITC Grenoble, France
W. M. Weber et al.
18-25 Mai 2015
Inviter: Prof. Olivier Thomas (Aix-Marseille Université, CNRS)

(16) Silicidation and Strain Analysis of Silicon Nanowires
2015 International Conference on Frontiers of Characterization and Metrology for Nanoelectronis (FCMN) Dresden, Germany
W. M. Weber et al.
14-16. April 2015

(15) Reconfigurable nanowire transistors: enhanced functionality driven by the unique properties of metal-semiconductor nano-junctions
International Conf. on Small Science ICSSCI,
8-11 Dec.2014 Hong Kong, China
W. M. Weber et al.

(14) Dopant free CMOS enabled by strain incorporation into silicon nanowires
13th International Workshop on Stress-Induced Phenomena in Microelectronics, Austin/TX, USA
W. M. Weber et al.
Inviter: Prof. Wong (UT-Austin)

(13) Reconfigurable Silicon Nanowire Devices and Circuits: Opportunities and Challenges
DATE 2013, Dresden, Germany
W. M. Weber et al.
27. March 2014
Inviter: Prof. Ian O´Connor (University of Lyon)

(12) Reconfigurable Nanowire Electronics – Device Principles and Circuit Prospects
ESSDERC 2013
W. M. Weber et al.
September 18. 2013, Bucharest, Romania

(11) Reconfigurable Nanowire Electronics – Device Principles and Prospects
Functionality-Enhanced Devices Workshop FEP
EPFL, March 25. 2013, Lausanne, Switzerland
W. M. Weber et al.
Inviters: G. de Micheli, P.-E. Gaillardon

(10) Reconfigurable Nanowire Electronics
Nanowires 2012 - Physics, Chemistry, and Applications of Semiconducting Nanowires, W. M. Weber et al.
September 20. 2012 Berlin, Germany

(09) Thermal treatment of silicon nanowires with Ni-silicide contacts
Subtherm 2011, November 2011 Dresden, Germany
W. M. Weber et al, Inviter: H. Schmidt

(08) Silicon/metal nanowire heterostructure synthesis and novel reprogrammable devices fabricated thereof
Freiberger Silizium Tage, Freiberg, Germany
Jun. 16 2011, Inviter: Prof. Johannes Heitmann

(07) Reconfigurable Nanowire Electronics
ECS Meeting 2011, Mai 2. 2011, Montreal, Canada
W. M. Weber et al.

(06) Polarity Controllable Silicon Nanowire Schottky Barrier Field Effect Transistors - A Building Block for Reconfigurable Systems
Nanofair 2010, July 7 2010. Dresden, Germany

(05) Polarity control of silicon nanowire transistors by electrostatic coupling to the Schottky contacts
DPG-Frühjahrstagung 2009, March 25 2009. Dresden, Germany.

(04) Tuning the Polarity of Silicon Nanowire FETs Evading Dopants
VDE-Kongress Zukunftstechnologien, *Nanoworkshop*, November 4. 2008, Munich, Germany.

(03) Tuning the Polarity of Silicon Nanowire Transistors without the use of Doping
IEEE Nanotechnology Conference, 2008, USA
W. M. Weber et. Al, Presenter Prof. P. Lugli

(02) Silicon Nanowire Transistors with Axially Intruded Nickel Silicide Contacts
Invited research lecture
XXI. IWEPNM 2007, Kirchberg, Austria, Inviter Prof. H. Kuzmany

(01) Silicon nanowires: catalytic growth and electrical characterization
Invited research lecture
W. M. Weber , G. Duesberg, F. Kreupl et. al
XX. IWPENM 2006 Kirchberg Austria, held by G. Duesberg

V. Invited Lectures & Seminar Talks

(26) Functionality Enhanced Nanoelectronics for Beyond CMOS Computing
NanoSyn-nanoNET Austria Meeting and Think Tank Erwin Schrödinger Gesellschaft
9. March 2020

(25) Emerging Nanoelectronic Devices
TU Dresden Faculty of Electrical Engineering and Information Technology
30 Nov. 2018

(24) Nanowire Electronics for Beyond CMOS Applications
17th. Dresden Microelectronics Academy – From Moore to Emerging Devices
17-21. September 2018

(23) Nano- and Quantum-Semiconductor Wires for Heterogeneously Integrated Logic and Sensor Systems
Faculty of Electrical and Computer Engineering, TU München, Munich, Germany
16. Mai 2018

(22) Innovation paths towards micro- and power-electronic systems
Faculty of Technical Sciences, University of Innsbruck, Austria
24. July 2017

(21) Reconfigurable Silicon and Germanium Nanowire Electronics – From Multifunctional Devices to Circuits
***Lund University, Department of Elec. and Information Technology**, Lund Sweden*
28 September 2015
Inviter: Prof. Lars-Erik Wernersson

(20) Reconfigurable Nanowire Electronics – Towards a Dopant Free Single MOS Technology
***LSI Seminar – EPFL, Lausanne**, Switzerland*
11 September 2015
Inviter: Prof. Giovanni de Micheli, Dr. Pierre-Emmanuel Gaillardon

(19) Nano-Inspired Microelectronic and Power-Electronic Innovations - from Materials to Systems
Faculty of Technical Sciences, University of Innsbruck, Austria
20. March 2015

(18) Nanowire Electronics
Nanonet Workshop, Rathen, Germany
29-30. September 2014

(17) Added value nanowire electronics
Dresden Microelectronics Academy – From Moore to Emerging Devices
6. September 2014

(16) Reconfigurable Nanowire Electronics – Device Principles and Prospects
Center for Advanced Electronics Dresden – Cluster of Excellence
Research Lecture at the Opening Festival of the cluster of excellence, Dresden, Germany
Feb. 28 2013
Inviter: Prof. Gerhard Fettweis

(15) Electronic transport in silicon – metal nanowire heterostructures
Leibniz Institute for Solid State and Materials Research (IFW)- Institute for Integrative Nanosciences, Dresden, Germany
Dec. 2 2011

(14) Reconfigurable electronics: Enhanced circuit functionality enabled by nanotechnology
POSTECH, World Class University, Convergence Engineering, Pohang, South-Korea
Nov. 23 2010
Inviters: Dr. Meyya Meyyappan, Prof. J.S-Lee

(13) Reconfigurable Silicon Nanowire Circuits, A Novel Approach for Future Electronics
7. Chemnitz Seminar for Nanotechnology , Nanomaterials and Nanoreliability
Fraunhofer Institute (ENAS) Chemnitz, Germany. Mai 24. 2011
Inviter: Prof. Stefan Schulz

(12) Silicon to Nickel Silicide Longitudinal Nanowire Heterostructures: Synthesis, Transport Properties Novel Devices and Circuits
TU-Dresden. Dresden, Germany. Mai 5. 2010
Inviter: Prof. Gianaurelio Cuniberti

(11) Silizium Nanodraht Elektronik: Erweiterte Funktionalität getrieben durch kleinste Strukturabmessungen
Fraunhofer Institut Werkstoff- und Strahltechnik (IWS). Dresden, Germany.
February 22. 2010
Inviter: Dr. Ines Dani

(10) Silicon to Nickel Silicide Longitudinal Nanowire Heterostructures: Synthesis, Transport Properties and Novel Devices
IBM Research - Zurich Research Labs. Rüschlikon, Switzerland.
March 20. 2009

(9) Silicon / nickel silicide nanowire heterostructures for high performance electronics
Institute for Nanoelectronics, TU-München, Munich Germany. *June 5. 2008*

(8) Silicon to nickel-silicide axial nanowire heterostructures for high performance electronics
TU Delft, Kavli Institute for Nanoscience, Quantum Transport Group.
Delft, The Netherlands. *September 3. 2007*
Inviter: Prof. L. P. Kouwenhoven

(7) Silicon to nickel-silicide axial nanowire heterostructures for high performance electronics
Philips Research Laboratory, Eindhoven, The Netherlands. *August 8. 2007*
Inviter: Dr. E.P.A.M. Bakkers

(6) Silicon / nickel-silicide axial nanowire heterostructures for high performance electronics
Cambridge University, U.K., CAPE-Lecture. *June 22. 2007*
Inviters: Prof. J. Robertson, Prof. A. Ferrari and Prof. S. Hoffmann.

(5) Non-linear saturation-current vs. gate length of silicon nanowire FETs
CEA, DRFMC Grenoble France. *February 26. 2007*
Inviters: Dr. S. Roche and Dr. Y. M. Niquet

(4) Growth and Electrical Characterization of Si/NiSi$_x$ Nanowire Heterostructures
Institute Talk. CNI, Forschungszentrum Jülich, Jülich Germany. *September 13. 2006*
Inviters: Prof. S. Mantl and Dr. J. Knoch

(3) Research on Semiconductor Nanowire Transistors at Qimonda
H. Riechert, W. M. Weber, C. Chéze, L. Geelhaar
Stanford University, Stanford CA, USA. *August. 2006.* Held by Dr. Henning Riechert
Inviter: Prof. James S. Harris

(2) Intrinsic Silicon Nanowires: Growth and Electrical Characterization
Institute for Nanoelectronics, TU-München, Munich Germany. *April 27. 2006*
Inviter: Prof. P. Lugli

(1) Application of silicon nanowires in microelectronics
Institute for Nanoelectronics, TU-München, Munich Germany. *Mai 19. 2005*
Inviter: Prof. P. Lugli

VI. Conference Contributions (selection):

(38) Size effect of electronic properties in highly arsenic-doped silicon nanowires
T. Mauersberger, I. Ibrahim, M. Grube A. Heinzig, T. Mikolajick, W. M.Weber
IEEE- ULIS-EUROSOI, Grenoble, France 2019

(37) Eliminating Charge Sharing in Clocked Logic Gates on the Device Level Employing Transistors with Multiple Independent Inputs
J. Trommer, M. Simon, S. Slesazeck, W. M. Weber and T. Mikolajick
IEEE ESSDERC, Kraków , Poland (September 2019)

(36) IPCEI Subcontracts Contributing to 22-FDX Add-on Functionalities at GF
S. Kolodinski, C. Mart, W. Weinreich, V. Sessi, J. Trommer, T. Chohan, H. Mulaosmanovic, W. M. Weber, S. Slesazeck, B. Peng., C. Esposito, Y. Zimmermann, M. Schröter, Xin Xu, P.V. Testa, C. Carta, F. Ellinger, S. Lehmann, M. Drescher and M. Wiatr
IEEE ESSDERC, Kraków , Poland (September 2019)

(35) Junction tuning by ferroelectric switching in silicon nanowire Schottky field effect transistors
V. Sessi, H. Mulaosmanovic, R. Hentschel, S. Pregl, T. Mikolajick and W. M. Weber
IEEE Nanotechnology Conference. (2018)
July 2018, Ireland

(34) Realization of in-situ arsenic-doping of CVD grown silicon nanowires
Poster
I. Ibrahim, R. Mendes, M. Grube, M. H. Rümmeli, T. Mikolajick and W. M. Weber
Nanowire-Week
Lund, Sweden

(33) A wired-AND transistor: Polarity controllable FET with multiple inputs
M. Simon, J. Trommer, B. Liang, D. Fischer, T. Baldauf, M. B. Khan, A. Heinzig, M. Knaut, Y. M. Georgiev, A. Erbe, J. W. Bartha, T. Mikolajick and W. M. Weber
76th Device Research Conference (DRC),
July 2018, Santa Barbara CA, USA,

(32) A Physical Synthesis Flow for Early Technology Evaluation of Silicon Nanowire based Reconfigurable FETs
S. Rai, A. Rupani, D. Walter, M. Raitza, A. Heinzig, T. Baldauf, J. Trommer, C. Mayr, W. M. Weber and A. Kumar
Design, Automation and Test in Europe (DATE) (2018)

(31) Reconfigurable NAND-NOR Circuits Fabricated by a CMOS Printing Technique
A. Heinzig, S. Pregl, J. Trommer, T. Mikolajick and W. M. Weber
Nanotechnology Materials and Devices Conference (*NMDC)*
December 2017 179-181 (2017)

(30) Human α-thrombin detection platform using aptamers on a silicon nanowire field-effect transistor
L. Römhildt, F. Zörgiebel, B. Ibarlucea, M. Vahdatzadeh, L. Baraban, G. Cuniberti, S. Pregl, W. M Weber, T. Mikolajick and J. Opitz
Power and Timing Modeling, Optimization and Simulation (PATMOS), 7th International Symposium on (2017)

(29) Realization of in-situ arsenic-doping of CVD grown silicon nanowires
Poster
I. Ibrahim, R. Mendes, M. Grube, M. H. Rümmeli, T. Mikolajick and W. M. Weber
Nanowire-Week 2017
Lund, Sweden

(28) A CMOS-based Silicon Nanowire Array for Biosensing Applications
V. Sessi, B. Ibarlucea, F. Seichepine, S. Klinghammer, S. Pregl, N. Szabo, A. Hierlemann, L. Baraban, G. Cuniberti, U. Frey, T. Mikolajick and W. M. Weber
Nano-Bio-Sensors Conf. (2017)

(27) Reconfigurable Germanium Transistors with Low Source-Drain Leakage for Secure and Energy-Efficient Doping-free Complementary Circuits
J. Trommer, A. Heinzig, S. Slesazeck, U. Mühle, M. Löffler, D. Walter, C. Mayr, T. Mikolajick and W. M. Weber
75th Device Research Conference (DRC) (2017)

(26) In-Depth Electrical Characterization of Carrier Transport in Ambipolar Si-NW Schottky-Barrier FETs
D.Y. Jeon, T. Baldauf, S. J. Park, S. Pregl, L. Baraban, G. Cuniberti, T. Mikolajick and W. M. Weber
47th *European Solid-State Device Research Conference ESSDERC* (2017)

(25) Exploiting transistor-level reconfiguration to optimize combinational circuits
M. Raitza, A. Kumar, M. Völp, D. Walter, J. Trommer, T. Mikolajick and W.M. Weber
Design and Test in Europe - DATE (2017)

(24) Bringing reconfigurable nanowire FETs to a logic circuits compatible process platform
M. Simon, A. Heinzig, J. Trommer, T. Baldauf, T. Mikolajick, W.M. Weber
Nanotechnology Materials and Devices Conference (NMDC), 2016

(23) Integrating Bottom-Up Grown Silicon Nanowires on a CMOS Chip to Realize High-Density Transistor Arrays for Chemical Sensing
V. Sessi, F. Seichepine, S. Pregl, N. Szabo, A. Hierlemann, T. Mikolajick, W. M. Weber and U. Frey
20th International Conference on Miniaturized Systems for Chemistry and Life Sciences (μ TAS) October 9-13,

(22) Reconfigurable Nanowire Transistors with Multiple Independent Gates for Efficient and Programmable Combinational Circuits
J. Trommer, M. Raitza, A. Heinzig, T.Baldauf, M. Völp, T. Mikolajick and W. M. Weber
DATE Design and Test in Europe (2016)

(21) Strain-Engineering for Improved Tunneling in Reconfigurable Silicon Nanowire Transistors
T. Baldauf, A. Heinzig, J. Trommer, T. Mikolajick and W. M. Weber
EUROSOI-ULIS (2016), Vienna Austria

(20) Effect of Independently Sized Gates on the Delay of Reconfigurable Silicon Nanowire Transistor Based Circuits
J. Trommer A. Heinzig, T. Baldauf, S. Slesazeck, T. Mikolajick and W. M. Weber
EUROSOI-ULIS (2015)

(19) Stability and Performance of Heterogeneous Anode Assemblies of Silicon Nanowires on Carbon Meshes for Lithium-Sulfur Battery Applications
A. Krause, J. Brueckner, S. Doerfler, F. M Wisser, H. Althues, M. Grube, J. Martin, J.Grothe, T. Mikolajick, W. M Weber
MRS Meeting 2015 (2015)

(18) In-Situ Investigations of Individual Nanowires within a FIB/SEM System
M. Löffler, S. Banerjee, J. Trommer, A. Heinzig, W. Weber, and E. Zschech
Microsc. Microanal. 20 (Suppl 3) 360-361 (2014)

(17) Doped nanocrystalline carbon electrodes for graphene and CNT FETs
Poster
W. M. Weber, A. P. Graham, M. Grobosch, F. Kreupl and T. Mikolajick
IWEPNM 2012, International Winterschool on the Electronic Properties of Novel Materials, Kirchberg, Austria

(16) Reprogrammable Nanowire Transistors and Circuits
Poster
W.M. Weber, A. Heinzig, D. Martin, S. Slezaseck and T. Mikolajick
ElecMol 2010, International Meeting on Molecular Electronics, December 6, 2010, Grenoble, France

(15) Silicon and Nickel-Silicide Nano Wires as Novel Anode Materials for Lithium Batteries
Poster
S. Jakschik, W. Weber, A. Ispas, A. Bund and T. Mikolajick
ISE 2010, Nice, France

(14) Silicon nanowire FETs with extended functionality and novel dopant-free circuits
Oral Presentation
W. M. Weber, A. Heinzig, M. Emmerling, M. Kamp, L. Geelhaar, H. Riechert and Th. Mikolajick
Workshop on Nanowire Electronics, September 23, 2009, Lund, Sweden.

(13) Ambipolar Transport in Si-Nanowire Transistors
Oral presentation by P. Lugli
W. M. Weber, L. Geelhaar, F. Kreupl, E. Unger, H. Riechert, G. Scarpa and P. Lugli. Presenter: P. Lugli.
Nanotech Conference & Expo 2009 NSTI & CTSI 2009, Nanoelectronics: Research & Applications -1, Mai 3-7 2009 Houston, Tx. USA.

(12) Tuning the Polarity of Si-Nanowire Transistors Without the Use of Doping
Oral presentation by P. Lugli
W. M. Weber, L. Geelhaar, F. Kreupl H. Riechert, L. Lamagna, M. Fanciulli, G. Scarpa and P. Lugli. Presenter: P. Lugli.
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(11) Intrinsic Si-nanowire transistors with tunable polarity
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(9) Silicon to nickel-silicide axial nanowire heterostructures for high performance electronics
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(8) Silicon / nickel-silicide axial nanowire heterostructures for high performance electronics
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(7) Epitaxial Growth of GaN Nanowires on Al2O3 (0001) by Molecular Beam Epitaxy,
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(6) Non-Linear Gate Length Dependence of On-Current in Si-Nanowire FETs
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(5) Selfadjusted Shortening of the Active Region of Si –Nanowire Field Effect Transistors by Diffusion of NiSi
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(4) Field effect transistors with silicon nanowires as active region
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(3) Silicon nanowires: catalytic growth and electrical characterization
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W. M. Weber, G. S. Duesberg, A. P. Graham, M. Liebau, E. Unger, C. Chèze, L. Geelhaar, P. Lugli, H. Riechert and F. Kreupl.
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(2) Thin silicon nanowires: catalytic CVD growth and transistors
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W.M. Weber, E. Unger, A. Graham, M. Liebau, G. Duesberg, L. Geelhaar, H. Riechert, W. Pamler, P. Lugli and F. Kreupl.
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(1) Electron beam lithography for nanometer-scale planar double-gate transistors
Oral Presentation
W. M. Weber, G. Ilicali, J. Kretz, L. Dreeskornfeld, W. Rösner, W. Hansch and L. Risch.
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VII. Granted Patents

(3) Tim Baldauf, André Heinzig, Walter M. Weber
Reconfigurable nanowire field effect transistor, a nanowire array and an integrated circuit thereof
US Pat. US20180012996A1
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(2) Tim Baldauf, André Heinzig, Walter M. Weber –
„**Rekonfigurierbarer Nanodraht-Feldeffekt-Transistor und dessen Herstellung sowie ein Nanodraht-Array und dessen Rekonfigurierung**“ DE102016111237B3
Granted German Patent 23.11.2017 , Priority: 21.06.2016

(1) Walter M. Weber
„**Galvanische Zelle**“ DE102013201307AB4
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